We claim:

1. A method of forming an H_2 passivation layer in an FeRAM, comprising:

preparing a silicon substrate;

depositing a layer of TiO_x thin film, where $0<x<2$, on a damascene structure;

plasma space etching of the TiO_x thin film to form a TiO_x sidewall;

annealing the TiO_x side wall thin film to form a TiO_2 thin film;

depositing a layer of ferroelectric material; and

metallizing the structure to form a FeRAM.

2. The method of claim 1 wherein said plasma space etching precedes said annealing.

3. The method of claim 1 wherein said annealing precedes said plasma space etching.

4. The method of claim 1 wherein said preparing a silicon substrate includes doping to form a P-type silicon wafer, including threshold adjustment ion implantation, STI and filling of the trenches so formed with oxide, growth of a gate oxide, deposition of a polysilicon layer, ion implantation to form an N^+ source and an drain; smoothing the oxide by CMP, and patterning and etching the polysilicon layer.

5. The method of claim 4 which includes, after said preparing depositing a layer of oxide; smoothing the oxide by CMP, stopping at the level of the polysilicon layer; depositing a larger size bottom electrode; depositing another layer of oxide by CVD and smoothing the lastly deposited oxide layer by CMP, stopping at the level of the bottom electrode; depositing another layer of oxide by CVD; and patterning and etching the oxide layers to form trench structures.

6. The method of claim 1wherein said plasma space etching of the TiO_x thin film includes setting TCP Rf power at about 370W, setting the bias power to about 130 W at a chamber pressure of about 5 torr; and using etching including BCl_3 at a flow rate of about 30 sccm and Cl_2 at a flow rate of about 58 sccm.

7. The method of claim 1wherein said depositing a layer of TiO_x thin film, where $0<x<2$, includes preparing a MOCVD precursor, including dissolving about 0.2 mol $Ti(OC_3H_7)_4$ in Octane, resulting in a precursor solution having a concentration of 0.2 mol $Ti(OC_3H_7)_4$.

8. The method of claim 7 which further includes injecting the precursor solution into a CVD chamber vaporizer at temperature in the range of between about 80°C to 120°C by a liquid controller at a rate of between about 0.1 ml/min to 0.5 ml/min to form a precursor gases; maintaining a CVD chamber feed line at a temperature of between about 80°C to 120°C; maintaining the deposition temperature at between about 380°C to 420°C; maintaining the deposition pressure at between about 0.5 torr to 5 torr, and continuing the deposition process for between about five minutes to thirty minutes.

9. A method of forming an H_2 passivation layer in an FeRAM, comprising:

preparing a silicon substrate;

depositing a layer of TiO_x thin film, where $0<x<2$, on a damascene structure;

plasma space etching of the TiO_x thin film to form a TiO_x sidewall;

annealing the TiO_x side wall thin film to form a TiO_2 thin film;

depositing a layer of ferroelectric material; and

metallizing the structure to form a FeRAM.

10. The method of claim 9 wherein said preparing a silicon substrate includes doping to form a P-type silicon wafer, including threshold adjustment ion implantation, STI and filling of the trenches so formed with oxide, growth of a gate oxide, deposition of a polysilicon layer, ion implantation to form an N^+ source and an drain; smoothing the oxide by CMP, and patterning and etching the polysilicon layer.

11. The method of claim 10 which includes, after said preparing depositing a layer of oxide; smoothing the oxide by CMP, stopping at the level of the polysilicon layer; depositing a larger size bottom electrode; depositing another layer of oxide by CVD and smoothing the lastly deposited oxide layer by CMP, stopping at the level of the bottom electrode; depositing another layer of oxide by CVD; and patterning and etching the oxide layers to form trench structures.

12. The method of claim 9 wherein said plasma space etching of the TiO_x thin film includes setting TCP Rf power at about 370W, setting the bias power to about 130 W at a chamber pressure of about 5 torr; and using etching including BCl_3 at a flow rate of about 30 sccm and Cl_2 at a flow rate of about 58 sccm.

13. The method of claim 9 wherein said depositing a layer of TiO_x thin film, where $0<x<2$, includes preparing a MOCVD precursor, including dissolving about 0.2 mol $Ti(OC_3H_7)_4$ in Octane, resulting in a precursor solution having a concentration of 0.2 mol $Ti(OC_3H_7)_4$.

14. The method of claim 13 which further includes injecting the precursor solution into a CVD chamber vaporizer at temperature in the range of between about 80°C to 120°C by a liquid controller at a rate of between about 0.1 ml/min to 0.5 ml/min to form a precursor gases; *maintaining a CVD chamber feed line at a temperature of between about 80°C to 120°C*; maintaining the deposition temperature at between about 380°C to 420°C; maintaining the deposition pressure at between about 0.5 torr to 5 torr, and continuing the deposition process for between about five minutes to thirty minutes.

15. A method of forming an H_2 passivation layer in an FeRAM, comprising:

preparing a silicon substrate;

depositing a layer of TiO_x thin film, where $0<x<2$, on a damascene structure;

annealing the TiO_x side wall thin film to form a TiO_2 thin film;

plasma space etching of the TiO_2 thin film to form a TiO_2 sidewall;

depositing a layer of ferroelectric material; and

metallizing the structure to form a FeRAM.

16. The method of claim 15 wherein said preparing a silicon substrate includes doping to form a P-type silicon wafer, including threshold adjustment ion implantation, STI and filling of the trenches so formed with oxide, growth of a gate oxide, deposition of a polysilicon layer, ion implantation to form an N^+ source and an drain; smoothing the oxide by CMP, and patterning and etching the polysilicon layer.

17. The method of claim 16 which includes, after said preparing depositing a layer of oxide; smoothing the oxide by CMP, stopping at the level of the polysilicon layer; depositing a larger size bottom electrode; depositing another layer of oxide by CVD and smoothing the lastly deposited oxide layer by CMP, stopping at the level of the bottom electrode; depositing another layer of oxide by CVD; and patterning and etching the oxide layers to form trench structures.

18. The method of claim 15 wherein said plasma space etching of the TiO_x thin film includes setting TCP Rf power at about 370W, setting the bias power to about 130 W at a chamber pressure of about 5 torr; and using etching including BCl_3 at a flow rate of about 30 sccm and Cl_2 at a flow rate of about 58 sccm.

19. The method of claim 15 wherein said depositing a layer of TiO_x thin film, where $0<x<2$, includes preparing a MOCVD precursor, including dissolving about 0.2 mol $Ti(OC_3H_7)_4$ in Octane, resulting in a precursor solution having a concentration of 0.2 mol $Ti(OC_3H_7)_4$.

20. The method of claim 19 which further includes injecting the precursor solution into a CVD chamber vaporizer at temperature in the range of between about 80°C to 120°C by a liquid controller at a rate of between about 0.1 ml/min to 0.5 ml/min to form a precursor gases; maintaining a CVD chamber feed line at a temperature of between about 80°C to 120°C; maintaining the deposition temperature at between about 380°C to 420°C; maintaining the deposition pressure at between about 0.5 torr to 5 torr, and continuing the deposition process for between about five minutes to thirty minutes.